WEST Search History

DATE: Wednesday, September 24, 2003

Set Name side by side	Query	Hit Count	Set Name result set
DB=JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ			
L9	profil$ and (hardware near3 counter)	5	L9
DB=USPT,PGPB; PLUR=YES; OP=ADJ			
L8	L5 and (counter near2 ID)	0	L8
L7	L5 and (branch$ near2 ID)	0	L7
L6	L5 and (instruction near2 ID)	2	L6
L5	L4 and edg$	104	L5
L4	profil$ and (hardware near3 counter)	216	L4
L3	L1 and profil$ and (hardware near3 counter)	18	L3
L2	L1 and profil$ and counter	157	L2
L1	((717/126 |717/127 |717/128 |717/129 |717/130 |717/131 |717/132 |717/133 |717/151 |717/158)!.CCLS.)	1118	L1

END OF SEARCH HISTORY

Search Results - Record(s) 1 through 5 of 5 returned.

☐ 1. Document ID: JP 02310705 A

L9: Entry 1 of 5 File: JPAB Dec 26, 1990

PUB-NO: JP402310705A
DOCUMENT-IDENTIFIER: JP 02310705 A
TITLE: RECONSTITUTABLE COUNTER AND ITS CONSTITUTION METHOD

PUBN-DATE: December 26, 1990

INVENTOR-INFORMATION:
NAME COUNTRY
CRUICKSHANK, ANCIL B
DAVIS, RICHARD K

INT-CL (IPC): G05B 19/05

ABSTRACT:

PURPOSE: To reconstitute a counter into one of several different hardware counter constitutions by a program by providing a memory where plural counter profiles corresponding to counter constitutions having different forms are stored.

CONSTITUTION: Plural different counter constitution parameter files are stored in a non-volatile memory 40 connected to a microprocessor 30. Various selectable user parameters for another model constitution of a selected counter profile are stored in a memory 45, and the memory 45 functions as a pointer, namely, a selector. The microprocessor 30 selects one of three counter constitution parameter files in the memory 40 in accordance with the command from an input device 35 and programs a reconfigurable counter part 25 into this selected counter constitution. Thus, the counter is reconstituted into one of several different hardware counter constitutions by the program.

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Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 2. Document ID: NN76053935

L9: Entry 2 of 5 File: TDBD May 1, 1976

TDB-ACC-NO: NN76053935

DISCLOSURE TITLE: Position Servo Utilizing Position Reference Clock. May 1976.

PUBLICATION-DATA:
IBM Technical Disclosure Bulletin, May 1976, US

VOLUME NUMBER: 18
ISSUE NUMBER: 12
PAGE NUMBER: 3935 - 3936

DISCLOSURE TEXT:

2p. The device and procedure described herein provides an implementation of a closed-loop servo system which can be made to follow some desired trajectory. - Fig. 1 is both an implementation of a hardware version and a microprocessor implementation. In Fig. 1, the circuits (shown in block diagram form) encircled by block 10 would be replaced by a microprocessor. Incidentally, block 10 is a representation of the microprocessor. - Fig. 2 is a sketch of the trajectory that the servo will follow. - The hardware implementation that makes up the drive signal to motor 14 is comprised of reference voltage path A, which is an open-loop branch whose purpose is to apply a precalculated voltage profile to motor 14 via amplifier 12. If all system parameters are at their nominal values, the reference voltage derived from reference voltage path A would alone drive the system along the desired trajectories. Positional error path 13 is derived from the closed-loop portion of the servo system, and its magnitude is proportional to the difference between the position reference and the actual output position. - Referring to Fig. 1, the feedback signals on terminal 16 and terminal 18 are digital information derived from a two-phase digital tachometer 20. The problem therefore is to develop a digital signal Pr(t) which is compatible with the digital system. - Fig. 3A shows a desired continuous output position trajectory denoted by Pdo(t). The vertical axis of the plot corresponds to position and has been divided into incremental position steps of Delta. Delta corresponds to the incremental position supplied by each cycle of the digital tachometer 20. Horizontal lines are drawn from each Delta on the vertical axis until the curve Pdo(t) is intersected. Another line is drawn vertically from the point of intersection to the horizontal axis which denotes time. - The sketch in Fig. 3B shows a train of pulses called Position Reference Clock which is derived from position reference clock generator 22. If the output of the servo did truly follow Pdo(t), then a full cycle of the digital tachometer would occur at each pulse location of the Position Reference Clock. Generation of the Position Reference Clock is then the desired reference, Pr(t), for the closed-loop position servo system. - Generation of the position can be either done in hardware or by use of a microprocessor. A hardware version is shown in Fig. 4. Essentially the hardware version consists of a counter, reference crystal clock, some logic and a read-only memory. The memory contains the periods T1, T2...Tn of the tachometer 20 corresponding to desired output trajectory. The control logic sequentially loads in T1, T2...Tn from the memory into the down counter after each position reference pulse is generated. When the counter reaches zero, it puts out a pulse which is Position Reference Clock and a new Tn is loaded into the counter to continue the process. Incidentally, all hardware could be a portion of a microprocessor.

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☐ 3. Document ID: US 20020019930 A1

L9: Entry 3 of 5 File: DWPI Feb 14, 2002

DERWENT-ACC-NO: 2002-216176
DERWENT-WEEK: 200227
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TITLE: Instruction profiling and trace selection system has hardware portion which detects more frequently executed instructions and software portion which forms trace of most frequently executed instructions

INVENTOR: BENITEZ, M; HSU, W C

PRIORITY-DATA: 1999US-0252567 (February 18, 1999), 2001US-0968283 (October 1, 2001)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 20020019930 A1	February 14, 2002		009	G06F009/00

INT-CL (IPC): G06 F 9/00

ABSTRACTED-PUB-NO: US20020019930A
BASIC-ABSTRACT:

NOVELTY - A hardware portion including counters and memory, detects which instructions of a program are more frequently executed and maintains a history of targets chosen by branch instructions of the program. A software portion forms the trace of the most frequently executed instructions and uses the maintained history in making branch predictions which are encountered in forming the trace.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for program instructions profiling method.

USE - For selecting profile instructions of a program and for selecting a trace of a portion of the instructions of the program.

ADVANTAGE - Uses the software which has more flexibility, less complexity and less expensive than hardware, for trace prediction and selection. Provides fast profiling and effective trace selection.

DESCRIPTION OF DRAWING(S) - The figure shows the trace selection mechanism.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Clip Img | Image

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☐ 4. Document ID: DE 10194944 T WO 200161499 A1 AU 200132543 A US 20010021959 A1

L9: Entry 4 of 5 File: DWPI Jun 12, 2003

DERWENT-ACC-NO: 2002-239485
DERWENT-WEEK: 200346
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TITLE: Processor system in computer, has hardware counters to measure performance characteristics of part entities of load module

INVENTOR: EGELAND, T; HOLMBERG, P A ; NORRMAN, P ; OESTEN, K ; JOHANSSON, L K ; JOHANSSON, L K O

PRIORITY-DATA: 2000SE-0000533 (February 18, 2000)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
DE 10194944 T	June 12, 2003		000	G06F012/08
WO 200161499 A1	August 23, 2001	E	044	G06F012/08
AU 200132543 A	August 27, 2001		000	G06F012/08
US 20010021959 A1	September 13, 2001		000	G06F012/00

INT-CL (IPC): G06 F 12/00; G06 F 12/08

ABSTRACTED-PUB-NO: US20010021959A
BASIC-ABSTRACT:

NOVELTY - Memory allocation sections (38,41,48) is updated during a run time based on execution data provided by an execution profiling section (39). The profiling section has hardware counters (51) to measure performance characteristics of part entities of load modules (49,50) which has record and instruction data. Memory allocation section allocates selected part entities of load module to memory.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for memory handling method.

USE - In computer.

ADVANTAGE - More important data are held in static cache or the necessary memory size is reduced by a fine granularity of the data by the static cache. The access times are reduced due to close arrangement to the processor. Increases the flexibility by intermittently updating the allocation based on execution profile measurements.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of processor system.

Memory allocation sections 38,41,48

Execution profiling section 39

Load modules 49,50

Hardware counters 51
ABSTRACTED-PUB-NO:

WO 200161499A EQUIVALENT-ABSTRACTS:

NOVELTY - Memory allocation sections (38,41,48) is updated during a run time based on execution data provided by an execution profiling section (39). The profiling section has hardware counters (51) to measure performance characteristics of part entities of load modules (49,50) which has record and instruction data. Memory allocation section allocates selected part entities of load module to memory.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for memory handling method.

USE - In computer.

ADVANTAGE - More important data are held in static cache or the necessary memory size is reduced by a fine granularity of the data by the static cache. The access times are reduced due to close arrangement to the processor. Increases the flexibility by intermittently updating the allocation based on execution profile measurements.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of processor system.

Memory allocation sections 38,41,48

Execution profiling section 39

Load modules 49,50

Hardware counters 51

☐ 5. Document ID: SU 1105916 A

L9: Entry 5 of 5 File: DWPI Jul 30, 1984

DERWENT-ACC-NO: 1985-060734
DERWENT-WEEK: 198510
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TITLE: Process control system moving hardware counter - has threshold forming signal triggering pulse generator at input to counter

INVENTOR: KOROTKOV, A V

PRIORITY-DATA: 1983SU-3590836 (May 10, 1983)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
SU 1105916 A	July 30, 1984		003	

INT-CL (IPC): G06M 7/00

ABSTRACTED-PUB-NO: SU 1105916A
BASIC-ABSTRACT:

Moving objects counter contg. the sensor (1), memory (5), comparator (7) and counter (8), has the threshold (2), pulse generator (3), counter (4) and the D/A converter (6).

As a detail passes through the sensor, the threshold forms a signal which triggers the pulse generator and so fills the counter. The memorised codes are obtained in quantising the data signal from the detail being registered. The memory presents consecutive codes which are converted into a stepped signal coinciding in shape with the signal from the detail. At coincidence the signal from the comparator is registered by the output counter.

USE/ADVANTAGE - In automatic counting of the output of automated process control systems, to identify details by the form of the sensor signal (the profile of the detail) as well as by the length of the detail, so increasing accuracy in differentiated counting of objects. Bul.28/30.7.84